What the invention claimed is:

1. A logic analyzer data retrieving method used in a logic analyzer comprised of a control unit, a memory unit, and a data retrieving circuit, said data retrieving circuit obtaining a qualified clock when received a clock signal and a clock qualifier signal, for enabling said control unit to catch test data from a test sample been connected thereto subject to said qualified clock and to store caught test data in said memory unit and then to transfer test data from said memory unit to the display screen of an external computer system for examination, the logic analyzer data retrieving method comprising the step of driving said data retrieving circuit to receive a time delay default value and to store said time delay default value in a buffer in a time delay circuit, and the step of triggering the preset of a first counter and transferring said default value from said buffer to said first counter to drive said first counter to start counting when a clock qualifier signal entered, so as to obtain a complete clock enable signal when said first counter counted up to said default value and the output of the clock enable became low.

2. The logic analyzer data retrieving method as claimed in claim 1, further comprising the step of triggering the reset of a second counter of said control circuit to cause said second counter to start counting till appearance of a next clock enable signal when

a complete clock enable ended, and the step of storing the value of said second counter in said memory unit when said second counter stopped the counting and then displaying the value on a display screen.

3. A logic analyzer data retrieving method used in a logic analyzer comprised of a control unit, a memory unit, a buffer, a display screen, and a data retrieving circuit, said data retrieving circuit obtaining a qualified clock when received a clock signal and a clock qualifier signal, for enabling said control unit to catch test data from a test sample been connected thereto subject to said qualified clock and to store caught test data in said memory unit and then to write test data from said memory unit to said buffer and to transfer test data from said buffer to said display screen for review, the logic analyzer data retrieving method comprising the step of driving said data retrieving circuit to receive a time delay default value and to store said time delay default value in a buffer in a time delay circuit, and the step of triggering the preset of a first counter and transferring said default value from said buffer to said first counter to drive said first counter to start counting when a clock qualifier signal entered, so as to obtain a complete clock enable signal when said first counter counted up to said default value and the output of the clock enable became low.

4. The logic analyzer data retrieving method as claimed in

claim 3, further comprising the step of triggering the reset of a second counter of said control circuit to cause said second counter to start counting till appearance of a next clock enable signal when a complete clock enable ended, and the step of storing the value of said second counter in said memory unit when said second counter stopped the counting and then displaying the value on a display screen.

5. The logic analyzer data retrieving method as claimed in claim 1, wherein said logic analyzer has a sampling clock input only during the period of clock enable signal.

6. The logic analyzer data retrieving method as claimed in claim 1, wherein the output of clock enable signal is low when said first counter starts counting, and the output of clock enable signal is high when said first counter counted up to said default value.

7. The logic analyzer data retrieving method as claimed in claim 3, wherein said logic analyzer has a sampling clock input only during the period of clock enable signal.

8. The logic analyzer data retrieving method as claimed in claim 3, wherein the output of clock enable signal is low when said first counter starts counting, and the output of clock enable signal is high when said first counter counted up to said default value.

9. A logic analyzer data retrieving circuit used in a logic analyzer comprising a control unit and a memory unit and adapted

to obtain a qualified clock when received a clock signal and a clock qualifier signal, for enabling said control unit to catch test data from a test sample been connected thereto subject to said qualified clock and to store caught test data in said memory unit and then to transfer test data from said memory unit to the display screen of an external computer system for examination when the memory space of said memory unit fully occupied, the logic analyzer data retrieving circuit comprising a trigger assembly logic circuit, a control circuit, a time delay circuit, and a gate, wherein said trigger assembly logic circuit is to select the test signal to be edge trigger or level trigger, and then pass the entered test signal to said trigger assembly logic circuit to provide a clock qualifier, and then to send said clock qualifier to a first counter of said time delay circuit; said control circuit is adapted to receive a preset time delay default value and to store said default value in a memory thereof, for enabling said default value to be transferred to a buffer of said time delay circuit; said time delay circuit comprises a buffer and a first counter and is adapted to trigger the preset of said first counter and to transfer the default value from said buffer to said first counter to start counting when a clock qualifier signal entered.

10. The logic analyzer data retrieving circuit as claimed in claim 9, wherein said control circuit further comprising a second counter connected between said gate and said memory of said time

delay circuit.

11. The logic analyzer data retrieving circuit as claimed in claim 9, wherein said trigger assembly logic circuit is capable of receiving multiple test signals from multiple test samples.

12. The logic analyzer data retrieving circuit as claimed in claim 9, wherein said gate is an AND gate.

13. The logic analyzer data retrieving circuit as claimed in claim 9, wherein said gate is an OR gate.

14. A logic analyzer data retrieving circuit used in a logic analyzer comprising a control unit, a buffer, a display screen, and a memory unit and adapted to obtain a qualified clock when received a clock signal and a clock qualifier signal, for enabling said control unit to catch test data from a test sample been connected thereto subject to said qualified clock and to store caught test data in said memory unit and then to transfer test data from said memory unit to said buffer when the memory space of said memory unit fully occupied, and then to transfer test data from said buffer to said display screen for review, the logic analyzer data retrieving circuit comprising a trigger assembly logic circuit, a control circuit, a time delay circuit, and a gate, wherein said trigger assembly logic circuit is to select the test signal to be edge trigger or level trigger, and then pass the entered test signal to said trigger assembly logic circuit to provide a clock qualifier, and then to send said clock

qualifier to a first counter of a time delay circuit thereof; said control circuit is adapted to receive a preset time delay default value and to store said default value in a memory thereof, for enabling said default value to be transferred to a buffer of said time delay circuit; said time delay circuit comprises a buffer and a first counter and is adapted to trigger the preset of said first counter and to transfer the default value from said buffer to said first counter to start counting when a clock qualifier signal entered.

15. The logic analyzer data retrieving circuit as claimed in claim 14, wherein said control circuit further comprising a second counter connected between said gate and said memory of said time delay circuit.

16. The logic analyzer data retrieving circuit as claimed in claim 14, wherein said trigger assembly logic circuit is capable of receiving multiple test signals from multiple test samples.

17. The logic analyzer data retrieving circuit as claimed in claim 14, wherein said gate is an AND gate.

18. The logic analyzer data retrieving circuit as claimed in claim 14, wherein said gate is an OR gate.